**AMENDMENTS TO THE SPECIFICATION**

Please amend the following paragraphs of the Specification as shown below:

[0024] FIG. 2 is a first flow chart 100 demonstrating conceptual operating steps for the autonomous memory checker 10 of FIG. 1. During the boot-time after reset, the autonomous memory checker 10 receives a signal to enter the initial memory reference mode 110 from the host. In the initial memory reference mode 110, autonomous memory checker 10 fetches specified contents from memory via the DMA controller 15 and generates 115 memory reference values through an authentication engine 20 for desired memory ~~location~~ locations or blocks. Typical authentication schemes include, but are not limited to, secure hash algorithm 1 (SHA-1) and message digest algorithm 5 (MD5). The memory reference value represents a distinct value for specific memory contents. Each memory reference value is stored 117 in the memory reference file 40 for later comparison. The processes 115 and 117 are repeated until the autonomous memory checker 10 receives another signal from the host to enter a runtime check mode 120.

[0025] In runtime check mode 120, an adjustable time randomizer initiates memory reference comparison 130. When timer module 35 wakes up the rest of the circuitry in autonomous memory checker 10, controller 25 signals DMA controller 15 to fetch memory contents from specified blocks and addresses. The fetched memory contents are fed into the authentication engine 20 to generate a runtime reference value. The runtime reference value is compared 140 with the stored value in memory reference file 40. The compared runtime and memory reference values correspond to identical memory blocks and addresses. If the runtime and memory reference values match, then processes 130 and 140 are repeated whenever the adjustable time randomizer initiates another memory reference comparison. If the memory reference values do not match 150, then autonomous memory checker 10 enters an error mode 155 and hardware actions are taken.

[0027] FIG. 3 is a system block diagram 200 showing an autonomous memory checker 205 coupled to a host processor 210. Autonomous memory checker 205 has a master bus 245 which is used to read data from an internal memory block 215 and external memory blocks 220 and 225. Autonomous memory checker 205 is programmed by the host processor 210 over slave bus 255. Autonomous memory checker 205 has a DMA capability and does not require any actions from host processor 210 once it has been programmed. If the write-read checks are implemented, autonomous memory checker 205 should also be able to write to memory blocks 215, 220, and 225.